

1        **CLAIMS:**

2            1.     A method of forming a structure over a semiconductor  
3     substrate, comprising:

4            forming a silicon dioxide containing layer across at least some of  
5     the substrate;

6            providing nitrogen within the silicon dioxide containing layer,  
7     substantially all of the nitrogen within the silicon dioxide being at least  
8     10Å above the substrate; and

9            after providing the nitrogen within the silicon dioxide containing  
10    layer, forming conductively doped silicon on the silicon dioxide layer.

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12           2.     The method of claim 1 wherein the silicon dioxide layer is  
13    at least 30Å thick, and wherein substantially all of the nitrogen is  
14    provided in the top 10Å of the silicon dioxide layer.

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16           3.     The method of claim 1 wherein the nitrogen is provided  
17    within the silicon dioxide layer from plasma activated nitrogen species.

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19           4.     The method of claim 1 wherein the nitrogen is provided  
20    within the silicon dioxide layer by remote plasma nitridization utilizing  
21    nitrogen species generated in a plasma that is at least about 12 inches  
22    from the substrate.  
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1           5.     The method of claim 1 wherein the nitrogen is provided  
2     within the silicon dioxide layer by remote plasma nitridization utilizing  
3     nitrogen species generated in a plasma that is at least about 12 inches  
4     from the substrate; the plasma being generated in a chamber from N<sub>2</sub>,  
5     at a power of from about 1500 watts to about 3000 watts, and a  
6     pressure of from about 0.5 Torr to about 3 Torr; the substrate not being  
7     biased relative to the plasma during provision of the nitrogen within the  
8     silicon dioxide layer.

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10           6.     The method of claim 5 wherein the substrate is maintained  
11     at a temperature of from about 550°C to about 1000°C during provision  
12     of the nitrogen within the silicon dioxide layer.

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14           7.     The method of claim 5 wherein the substrate is exposed to  
15     the nitrogen species for a time of from greater than 0 minutes to about  
16     about 5 minutes.

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18           8.     The method of claim 1 wherein the nitrogen is provided  
19     within the silicon dioxide layer by plasma nitridization utilizing nitrogen  
20     species generated in a plasma that is at least about 4 inches from the  
21     substrate.

1           9.     The method of claim 8 wherein the substrate is maintained  
2     at a temperature of from about 550°C to about 1000°C during provision  
3     of the nitrogen within the silicon dioxide layer.

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5           10.    The method of claim 8 wherein the substrate is exposed to  
6     the nitrogen species for a time of from greater than 0 minutes to about  
7     about 5 minutes.

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9           11.    A method of forming structures over a semiconductor  
10    substrate, comprising:

11         forming a first oxide region which covers only a portion of the  
12         substrate;

13         providing nitrogen within the first oxide region, substantially all of  
14         the nitrogen within the first oxide region being at least 10Å above the  
15         substrate;

16         forming a second oxide region over at least some of the substrate  
17         which is not covered by the first oxide region;

18         forming a first conductively-doped silicon material over the first  
19         oxide region and a second conductively-doped silicon material over the  
20         second oxide region; one of the first and second conductively-doped  
21         silicon materials being n-type doped and the other being p-type doped.

1           12. The method of claim 11 wherein the nitrogen is provided  
2 within the first oxide region from plasma activated nitrogen species.

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4           13. The method of claim 11 wherein the second oxide region is  
5 thicker than the first oxide region.

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7           14. The method of claim 11 wherein the p-type doped silicon  
8 material is formed over the first oxide region.

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10          15. The method of claim 11 wherein the p-type doped silicon  
11 material is formed over the first oxide region, and is formed before  
12 forming the second oxide region.

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14          16. The method of claim 15 wherein the second oxide region is  
15 formed by oxidizing the substrate, and wherein the oxidizing also oxidizes  
16 the p-type doped silicon material to form a third oxide region over the  
17 p-type doped silicon material.

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17. The method of claim 11 wherein:

the p-type doped silicon material is formed over the first oxide region, and is formed before forming the second oxide region;

the second oxide region is formed by oxidizing the substrate, and wherein the oxidizing also the oxidizes the p-type doped silicon material to form a third oxide region over the p-type doped silicon material; and

the n-type doped silicon material is formed over the second and third oxide regions.

18. The method of claim 17 further comprising removing the n-type doped silicon material and third oxide layer from over the p-type doped silicon material.

19. The method of claim 17 further comprising removing the n-type doped silicon material and third oxide layer from over the p-type doped silicon material by chemical-mechanical planarization.

1           20.    The method of claim 17 further comprising:  
2                removing the n-type doped silicon material and third oxide layer  
3                from over the p-type doped silicon material;  
4                patterning the p-type doped silicon material into a first transistor  
5                gate;  
6                patterning the n-type doped silicon material into a second transistor  
7                gate;  
8                forming first source/drain regions proximate the first transistor gate  
9                to define a first transistor comprising the first source/drain regions and  
10              first transistor gate; and  
11              forming second source/drain regions proximate the second transistor  
12              gate to define a second transistor comprising the first source/drain  
13              regions and first transistor gate.

1           21. A method of forming a pair of transistors associated with a  
2 semiconductor substrate, comprising:

3           defining a first region and a second region of the substrate;

4           forming a first oxide region which covers at least some of the first  
5 region of the substrate and which does not cover the second region of  
6 the substrate;

7           providing nitrogen within the first oxide region;

8           after providing the nitrogen within the first oxide region, forming  
9 a first conductive layer over the first oxide region and which does not  
10 cover the second region of the substrate;

11          after forming the first conductive layer, forming a second oxide  
12 region over the second region of the substrate;

13          forming a second conductive layer over the second oxide region;

14          patterning the first conductive layer into a first transistor gate;

15          patterning the second conductive layer into a second transistor  
16 gate;

17          forming first source/drain regions proximate the first transistor gate  
18 and gatedly connected to one another by the first transistor gate; and

19          forming second source/drain regions proximate the second transistor  
20 gate and gatedly connected to one another by the second transistor gate.  
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1           22.    The method of claim 21 wherein the second oxide region is  
2 thicker than the first oxide region.

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4           23.    The method of claim 21 wherein the first and second  
5 conductive layers comprise conductively doped silicon.

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7           24.    The method of claim 21 wherein the first and second  
8 conductive layers comprise conductively doped silicon, the first conductive  
9 layer comprising p-type doped silicon and the second conductive layer  
10 comprising n-type doped silicon.

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12           25.    The method of claim 21 wherein the first and second  
13 conductive layers comprise conductively doped silicon, wherein the  
14 substrate is oxidized to form the second oxide region, and wherein the  
15 first conductive layer is oxidized during formation of the second oxide  
16 region.



1           26. The method of claim 21 wherein the first and second  
2       conductive layers comprise conductively doped silicon, wherein the  
3       substrate is oxidized to form the second oxide region, wherein the first  
4       conductive layer is oxidized during formation of the second oxide region,  
5       wherein the second conductive layer is formed over the oxidized first  
6       conductive layer; and wherein the second conductive layer is removed  
7       from over the oxidized first conductive layer prior to patterning the first  
8       conductive layer into a transistor gate.

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10           27. The method of claim 21 wherein the nitrogen is provided  
11       within the first oxide region from plasma activated nitrogen species.

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13           28. The method of claim 21 wherein the second oxide region is  
14       thicker than the first oxide region.

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16           29. The method of claim 21 wherein the p-type doped silicon  
17       material is provided over the first oxide region.

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19           30. The method of claim 21 wherein the p-type doped silicon  
20       material is formed over the first oxide region, and is formed before  
21       forming the second oxide region.

1           31. The method of claim 21 wherein the substrate comprises  
2 monocrystalline silicon and the oxide regions comprise silicon dioxide;  
3 and wherein the first and second oxide regions are grown from the  
4 monocrystalline silicon substrate.

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6           32. A semiconductor assembly, comprising:

7           a semiconductor substrate having a first region and a second region  
8 defined therein;

9           a first oxide region on the substrate and covering the first region  
10 of the substrate; the first oxide region having nitrogen provided therein;  
11 substantially all of the nitrogen being at least 10Å above the  
12 semiconductor substrate;

13           a first conductive layer over the first oxide region and defining a  
14 first transistor gate;

15           first source/drain regions proximate the first transistor gate and  
16 gatedly connected to one another by the first transistor gate; and

17           a second oxide region covering the second region of the substrate;

18           a second conductive layer over the second oxide region and  
19 defining a second transistor gate;

20           second source/drain regions proximate the second transistor gate  
21 and gatedly connected to one another by the second transistor gate.  
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1           33. The assembly of claim 32 wherein substantially all of the  
2 nitrogen is within a top 10Å of the first oxide region.

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4           34. The assembly of claim 32 wherein the second oxide region  
5 is thicker than the first oxide region.

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7           35. The assembly of claim 32 wherein the first conductive layer  
8 comprises p-type doped silicon and the second conductive layer comprises  
9 n-type doped silicon.